

PX2816B

Protocol Exerciser

エキサイザ部はI3CやI²C等のコントローラ/ターゲット等を構成できて動作時にはロジアナ機能で信号波形キャプチャとプロトコルデコードができる。信号発生と解析機能が一体化した新ツール。LA/PAオプション部は、16chのロジアナ/プロアナとして既存機種で実績のある機能を提供する。詳細な製品構成については立野電脳(株)へお問い合わせください。



Protocol Exerciser Main Device

- Data Transmission: USB 3.0 Type-C Interface
- Solid-State Drive (SSD) Storage Support
 - Users need to purchase and install a compatible M.2 2280 PCIe Gen3 or higher SSD.
 - SSD is used only in Logic Analyzer / Protocol Analyzer mode.

Protocol Exerciser Option: (including MIPI I3C, I²C, UART)

- 8 channels
- Capable of simulating protocol signals, configurable as Controller or Target device.
- Can edit topology of internal devices, where each device has separate settings.
- Can edit bus output voltage and operating modes.
- Controller Mode Simulation
 - Provides Quick settings (Template) for rapid script generation and editing.
 - Provides Design wizard for editing transmission protocol data.
- Target Mode Simulation
 - Supports different Target types in various different communication protocols.
- SDK Mode
 - Supports Python Automation control API and examples.
- Logic Analysis / Protocol Analysis Functions
 - Maximum sampling rate: 2 GHz.
 - With exerciser, enables simultaneous waveform observation and analysis.
 - Includes protocol decode and analyzer functions with packet statistics report.
- Power Supply and Power Consumption Measurement
 - Provides one DC power output (0.1–5 V) with simultaneous power consumption measurement.
- General Purpose Input/Output (GPIO): Two sets of GPIO ports.

Logic Analyzer Option (including Protocol Analyzer)

- 16 channels, 2 GHz timing analysis and 8-state protocol clause triggering.
- Supports detailed packet parsing, data and error statistics.
- Supports protocol packet/error triggering with customizable report view (show/hide columns).
- Real-time data search, waveform search (width / value / decode) and multi-column regex search.
- Multi-protocol decode with custom report output and integrated bus-decode waveform view.
- Overlay display with oscilloscope.
- 100+ protocol decodes, 20+ protocol triggers, and 20+ protocol analyzers

Main Device Packing List:



PX2816B Unit



USB 3.0 Cable



PD to DC
Adapter Cable



Power Adapter
(PD, 15V/3A)



Stack Cable*2



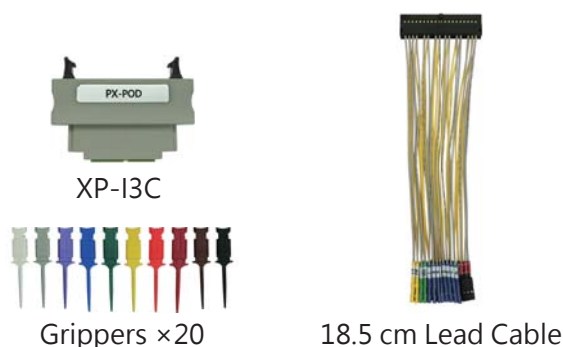
Protocol Exerciser Option - Specifications

Configurable Nodes	Supports 4 types: Controller, MIPI I3C Target, I ² C Legacy Target, Stress-Test Node
Packet Capture	Supports real-time MIPI I3C analysis with waveform and report Error and address packet statistics
Packets & Commands	Supports custom MIPI I3C and I ² C legacy packets Supports HDR-DDR mode Supports Hot-Join and In-Band Interrupt (IBI) Supports import/export of packets in JSON format
Topology Configuration	Custom dynamic address assignment strategy Display external and internal node information
SCL Frequency	Legacy I ² C: 50 KHz ~ 1 MHz Push-pull output: 100 KHz ~ 13 MHz Open-drain output: 100 KHz ~ 2.5 MHz
Pull-Up Resistance	100 Ω ~ 100 KΩ
Configurable Voltage Drive	I/O voltage range: 1 V ~ 5 V (resolution: 1 mV; accuracy: ±100 mV)
DC Output Voltage	Output voltage range: 1 V ~ 5 V (resolution: 10 mV; accuracy: ±100 mV)
Timing Resolution	5 ns
Error Injection	MIPI I3C S0–S5 errors as defined in the specification Custom CRC errors in HDR-DDR transfers Custom Preamble errors in HDR-DDR transfers Insert abnormal SDR packets in HDR-DDR transfers Reserved CCC values
API Support	Supports Python Automation control API (including topology configuration)

Logic Analyzer Option - Specifications

Storage Mode	On-board buffer: 4 Gb built-in DDR Real-time protocol data transfer to PC RAM (with decode) Real-time protocol data transfer to PC hard drive (long-duration recording) *Direct recording to device SSD — Users must purchase standard M.2 2280 PCIe SSD and install in slot on the bottom of the device
Supported Protocols	10BASE-T1S, BiSS-C, CAN2.0B/CAN FD, DALI, DP_Aux, eSPI, HID over I2C, I2C, I2S, LIN2.2, MDIO, MII, MIPI I3C 1.1.1, MIPI RFFE 3, MIPI SPMI 2, Modbus, PMBus, Profibus, RGMII, RMII, SMBus, SPI, SVID, UART, USB PD 3.1, USB1.1

Protocol Exerciser Option:



Logic Analyzer Option:

