November 2010

ProcStarIII™

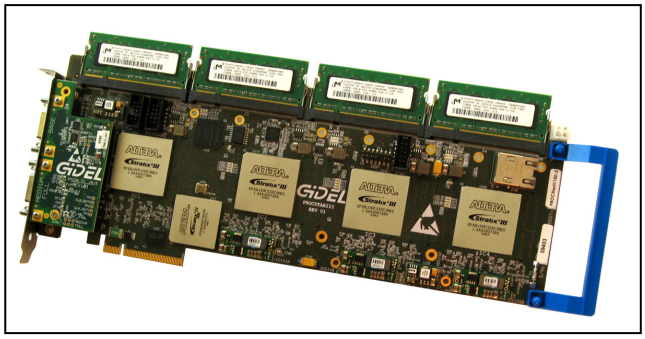
PCIe x8 Computation Accelerator

Key Features

- Up to 4 Stratix III 80E, 110E, 260E, 150L or 340L FPGAs
- 8-lane PCI Express (PCIe x8) host interface
- Five level memory structure (**33GB**+).
  Maximum sustain throughput of **12,000GB/s** to internal memories and **40GB/s** to DRAMs as follows:
  - ✓ Up to 4160 M9K (9K-bit) DPRAM blocks (4.6MB with **11,000GB/s** throughput @ 300Mhz)
  - ✓ Up to 192 M144K (144K-bit) RAM blocks (3.4MB with **1,000GB/s** throughput @ 300Mhz)
  - ✓ Up to 27,000 MLAB (640-bit) RAM blocks
  - ✓ Up to 4 large 256MB (optional 512MB) DDR2 memories with **16GB/s** sustain throughput using up to 24 ports. (Up to 64 ports with lower access rate)
  - ✓ 8 DDR2 SODIMMs with up to 4GB each at a maximum sustain throughput of **24 GB/s** using up to 64 ports.
- Supports 5 ProcStar III Daughter Boards (PSDB): Camera Links, User's Ethernet and other interfaces
- Up to 4 PSDB_DSP with 3 TI DSPs
- Typical system frequencies: 100-325 MHz.
- Flexible clocking system.
- Volatile and non volatile design security
- Reference design for fast direct board to board connection via SODIMM sockets.
- Supported by GiDEL's ***Proc Developer's Kit***s.

Benefits

- Leading edge performance
- Maximum flexibility to fit customer needs
- Cuts development cycle time and budget
- Maintainability
- Reliability
- Long life cycle



ProcStarIII *Board with one Daughter board and 4*SODIMMs*

Overview

The ***ProcStarIII***™ system provides a high-capacity, high-speed FPGA-based platform fortified with high throughput and massive memory resulting in a powerful and highly flexible system. The ***ProcStarIII*** can be hosted via 8-lane PCI Express. The performance, memory and add-on daughter boards' flexible architecture enable the system to meet almost any computation needs. In addition to 1GB on-board memory, eight SODIMM sockets provide up to 64GB of memory or additional connectivity and logic. Abundant memory conjoined with fast PCIe connection enable strong co-processing between a standard PC operating system and the FPGA acceleration.

The ***ProcStarIII*** system, with GiDEL's ***ProcDeveloper's Kit*** and tools, offers an incredible performance yet supports quick implementation of your unique design. It is done by eliminating the need for a high-speed board design, a PCI Express application driver, board constraints and environment FPGA code. The generated HDL code enables high throughput, easy-to-use parallel access to large memories. As a result, designers can focus on their proprietary value-added design. User designs may be in HDL, C-based, Simulink (graphical design) or any combination of them.

Development Environment

The ***ProcDeveloper's Kit,*** GiDEL's intuitive design and debug environment, facilitates design development effort on the ***ProcStarIII*** system. The kit contains ***ProcWizard***™, ***ProcMultiPort***™ IPs, ***PSDB_Proto***™, ***Quartus*** and ***USBBlaster***, and a ***ProcHILs***™ option.

The ***ProcWizard*** performs hardware initialization and automatically generates the following:

- Interface documentation in HTML or Microsoft Word
- C++ class(es) application driver(s) enable simultaneous accesses of multiple applications, each to its' dedicated section of the Proc board.
- Top-level designs, interface modules / entities and on-board memory controllers for the application use.
- Device constraints (as pin-outs).

The ***ProcMultiPort*** core IPs provides simple access as FIFOs and frame delays to the on-board DRAM. It enables parallel access to the on-board memory while enabling to split the physical memory into multiple logical memories. As a result the main benefits are:

- Simplifies design and enhances system performance
- Replaces the need for inventory of special memories by using standard memory and IP

The ***USBBlaster*** enables visibility of internal signals using the available FPGA memory.

The ***PSDB_Proto*** daughter board includes logic analyzer connections and prototyping area that enable rapid system additions via wiring/soldering devices and connectors.

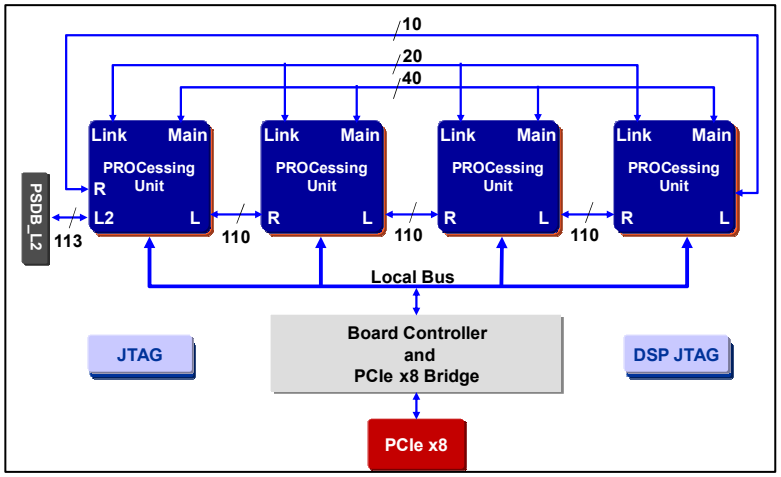
Processing Performance examples

Algorithm	Data flow rate	% critical resource of Stratix III logic		
		80E	110E	150L
1024*1024 FFT Width 12 bit Transform time 5.7mS	370 MHz	11%	8.2%	10%
9*9 filter symmetric **12** bit data **16** bit coefficients	336 MB/s	1%	<1%	<1%
7*7 8bit Median filter	255 MHz	11%	8.4%	6.3%
Circle open / close with radius up to 15 pixels 8 bit per pixel	323 MHz	5%	3.8%	2.9%
Threshold, add, subtract, 10→ 8 LUT,	>> 640 MHz	<< 1%	<< 1%	<< 1%

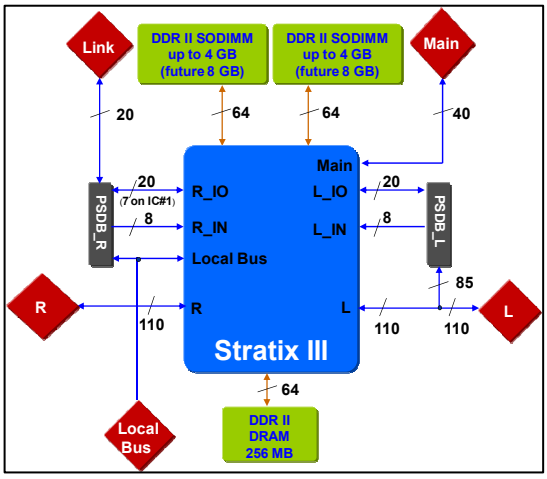
* Due to the different resource usage, better utilization is expected in a full design.

* For faster operation, use a multi-channel design.

* For 260 and 340L performance data, contact GiDEL.



ProcStarIII Board Diagram



Processing unit (FPGA, memories & connections)

Worldwide:
2 Ha'ilan Street, P.O. Box 281
Or Akiva, 30600, Israel
Tel: +972 - 4610 – 2500
Fax: +972 - 4610 - 2501
Email: sales_eu@gidel.com

Japan:
5-955 Baigo, Ome
Tokyo 198-0063 Japan
Tel: +81-(0)428-77-7000
Fax: +81-(0)428-77-7010
Email: sales@dsp-tdi.com

www.gidel.com

立野電脳 EXT営業部
E-mail : sales@dsp-tdi.com
〒198-0063 東京都青梅市梅郷5-955 TEL.0428-77-7000 FAX.0428-77-7010

URL http : //www.dsp-tdi.com/