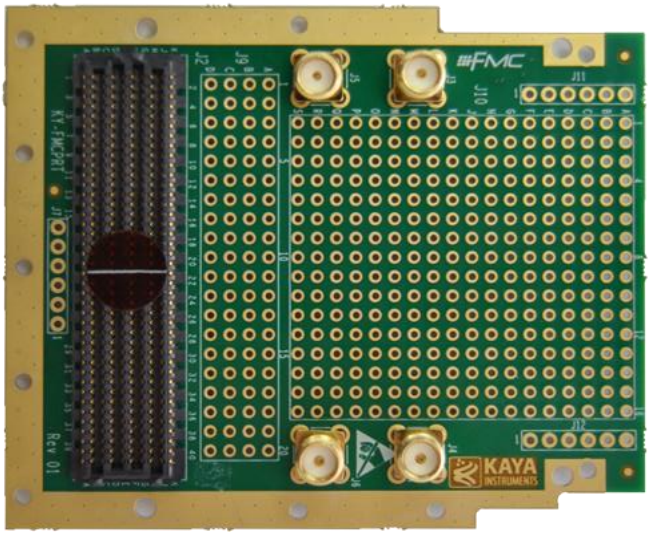
KAYA INSTRUMENTS

FPGA Mezzanine Card (FMC) prototype board (KY-FMC_PRT)

Overview

The FMC prototype board breaks out the complete LA bank of signals from the standard FMC Low Pin count Connector and the standard power rail and control signals. The user can add standard 0.1 inch spaced components and sockets for a wide variety of active and passive devices thus enabling the development of very complex capabilities. Standard control signals are available for the user to complete the interface to the chosen carrier card.



Features

- VITA 57.1 FMC compliant
- Passive breakout of Low Pin count Connector (LPC) pins to 0.1” matrix grid for soldering or wire-wrapping
- Development 18x16 hole matrix
- Extended Ground rails and Power breakout for two power connections
- JTAG breakout available in development matrix
- 4 SMA connectors for high speed serial signals (SerDes)
- User determined V_{ADJ} and V_{ref}
- 125MHz SerDes reference clock
- Control signals available for user connections in development matrix
- On board electrically erasable programmable memory, EEPROM, with 1Kb (128bytes) storage for configuration management and user data
- Supports air and conduction cooling FMC
- Single slot FMC
- -40°C to 85°C operating environment temperature (industrial grade)

About FMC

FPGA mezzanine card, or FMC, as defined in VITA 57.1, provides a specification describing an I/O mezzanine module with connection to an FPGA or other device with reconfigurable I/O capability. The FMC standard describes a versatile module, which can target a range of applications, environments, and markets. The specification defines a commercial grade version, which extends to cover a ruggedized conduction variant. FPGA's provide a high pin count that can operate at many Gbps. The latest connector technology is defined to maintain the high performance interface from the I/O on the mezzanine module, to the FPGA on the carrier card. The FMC mezzanine module design minimizes design effort and resources through minimal system support and flexible pin allocation.

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Applications

- ✓ Provides rapid means to develop new and complex FMC systems for later integration to standard FMC form factor
- ✓ Footprint for on board EEPROM simplifies complete FMC compatible interface
- ✓ Breakout of High Speed serial interfaces, clocks and control signals enables easy completion of full capability FMC functions

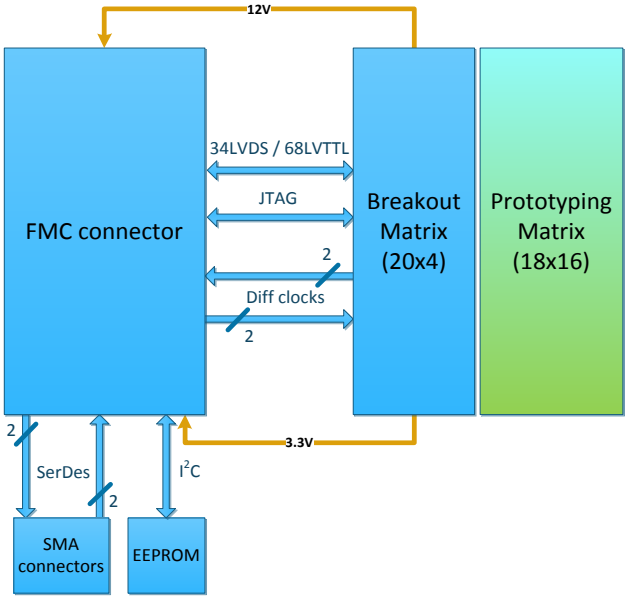
Ruggedization

The FMC prototype board is delivered in air and conduction cooled FMC standards. The board supports standard VITA 47 ruggedized levels for severe environmental conditions.

Deliverables

- FMC prototype board (KY-FMC_PRT)
- Hardware user manual

Block Diagram



参考：
FMCのピンと基板スルーホール、SMAへの接続表

Pin on Break Out Matrix	Signal on Break Out Matrix	Pin on FMC	Signal on FMC	Pin on Break Out Matrix	Signal on Break Out Matrix	Pin on FMC	Signal on FMC
A1	A1	G3	CLK0_C2M_N	C11	C11	H23	LA19_N
B1	B1	G2	CLK0_C2M_P	D11	D11	H22	LA19_P
C1	C1	H5	CLK0_M2C_N	A12	A12	G22	LA20_N
D1	D1	H4	CLK0_M2C_P	B12	B12	G21	LA20_P
A2	A2	G7	LA00_N_CC	C12	C12	H26	LA21_N
B2	B2	G6	LA00_P_CC	D12	D12	H25	LA21_P
C2	C2	D9	LA01_N_CC	A13	A13	G25	LA22_N
D2	D2	D8	LA01_P_CC	B13	B13	G24	LA22_P
A3	A3	H8	LA02_N	C13	C13	D24	LA23_N
B3	B3	H7	LA02_P	D13	D13	D23	LA23_P
C3	C3	G10	LA03_N	A14	A14	H29	LA24_N
D3	D3	G9	LA03_P	B14	B14	H28	LA24_P
A4	A4	H11	LA04_N	C14	C14	G28	LA25_N
B4	B4	H10	LA04_P	D14	D14	G27	LA25_P
C4	C4	D12	LA05_N	A15	A15	D27	LA26_N
D4	D4	D11	LA05_P	B15	B15	D26	LA26_P
A5	A5	C11	LA06_N	C15	C15	C27	LA27_N
B5	B5	C10	LA06_P	D15	D15	C26	LA27_P
C5	C5	H14	LA07_N	A16	A16	H32	LA28_N
D5	D5	H13	LA07_P	B16	B16	H31	LA28_P
A6	A6	G13	LA08_N	C16	C16	G31	LA29_N
B6	B6	G12	LA08_P	D16	D16	G30	LA29_P
C6	C6	D15	LA09_N	A17	A17	H35	LA30_N
D6	D6	D14	LA09_P	B17	B17	H34	LA30_P
A7	A7	C15	LA10_N	C17	C17	G34	LA31_N
B7	B7	C14	LA10_P	D17	D17	G33	LA31_P
C7	C7	H17	LA11_N	A18	A18	H38	LA32_N
D7	D7	H16	LA11_P	B18	B18	H37	LA32_P
A8	A8	G16	LA12_N	C18	C18	G37	LA33_N
B8	B8	G15	LA12_P	D18	D18	G36	LA33_P
C8	C8	D18	LA13_N	A19	A19	D34	TRST_L
D8	D8	D17	LA13_P	B19	B19	D33	TMS
A9	A9	C19	LA14_N	C19	C19	D31	TDO
B9	B9	C18	LA14_P	D19	D19	D30	TDI
C9	C9	H20	LA15_N	A20	A20	D29	TCK
D9	D9	H19	LA15_P	B20	B20	H40	VADJ
A10	A10	G19	LA16_N	C20	C20	H1	VREF_A_M2C
B10	B10	G18	LA16_P	D20	D20	A37	GND
C10	C10	D21	LA17_N_CC	J4	SMA_CON	C7	DP0_M2C_N
D10	D10	D20	LA17_P_CC	J6	SMA_CON	C6	DP0_M2C_P
A11	A11	C23	LA18_N_CC	J3	SMA_CON	C3	DP0_C2M_N
B11	B11	C22	LA18_P_CC	J5	SMA_CON	C2	DP0_C2M_P