KAYA VISION

CoaXPress v2.0 Device IP Datasheet

CoaXPress
Multi-Link Device FPGA IP Core

Innovative Approach

CoaXPress is a new digital transmission standard that supports the Gen<i>Cam international standard, providing a generic programming interface for all kinds of cameras regard-less of the interface technology. It also supports all Gen<i>Cam compliant image formats, including both rectangular and arbitrary shapes, area scan, line scan, multi ROIs and all standard pixel formats.

Each CoaXPress link supports up to 12.5 Gbps data rates, along with device power up to 13 W and device control at up to 41.6 Mbps – all on a single coax cable. For very fast devices, the links can be aggregated to provide multiples of the single coax bandwidth. Long cable lengths are supported – up to 30 meters at 12.5 Gbps and over 100 meters at 3.125 Gbps.

Key Features

- Compliant with CoaXPress v2.0 standard (JIIA NIF-001-2019) and backwards compatible with the V1.1 standard (JIIA NIF-001-2013)
- Support of up to 12.5 Gbps high speed-link and up to 41.6 Mbps low-speed link
- Multiple link rates support
- Versatile control channel operation with simple local bus without any CPU requirement
- Support of up to 4 CoaxPress links for targeting high throughput (extra links can be added per user request)
- Support of multiple video streams for applications based on multiple sensors or multi-tap sensors
- Highly configurable video streaming interface for enabling direct connection to imaging sensor
- Support video input of up to 16 pixels of 16-bit in parallel per clock
- Internal packer that implements the entire pixel packing schemes complying with JIIA NIF-001-2013 and later
- Embedded CRC-32 generator/check for streaming data packets
- Real-time behavior with low latency transmission
- Is provided with operational transceivers

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APPLICATIONS

- ✓ High speed cameras
- ✓ High definition cameras
- ✓ Panoramic cameras
- ✓ Upgrade for legacy coax based systems
- ✓ Defense remote systems
- ✓ Slip Ring systems
- ✓ Automotive surround view system
- ✓ Surveillance
- ✓ Robotic Vision

DEVICE SUPPORT

The following tables elaborate on the FPGA devices supported by the Device CXP IP. The Device CXP IP is provided with a reference design as standard which is based on the off-the-shelf evaluation board of the relevant FPGA vendor.
The reference design serves as an example design and targets to ease the integration and development process for contributing to cost reduction and improving time effectiveness.

Xilinx AMD FPGA

Device Family	Support	Maximum Links Speed	Evaluation Boards Reference Design	Code Options
Artix 7	CXP2.0	6.25Gbps	AC701	Encrypted netlist, Source code
Artix Ultrascale +	CXP2.0	12.5Gbps	Available on request	Encrypted netlist, Source code
Kintex 7	CXP2.0	12.5Gbps	KC705	Encrypted netlist, Source code
Kintex Ultra Scale	CXP2.0	12.5Gbps	KCU105	Encrypted netlist, Source code
Kintex Ultra Scale +	CXP2.0	12.5Gbps	KCU116	Encrypted netlist, Source code
ZYNQ 7000	CXP2.0	12.5Gbps	ZC706	Encrypted netlist, Source code
ZYNQ Ultra Scale +	CXP2.0	12.5Gbps	ZCU102/ZCU111	Encrypted netlist, Source code
Virtex 7	CXP2.0	12.5Gbps	VC709	Encrypted netlist, Source code
Virtex 7 Ultra Scale	CXP2.0	12.5Gbps	VCU108	Encrypted netlist, Source code
Virtex 7 Ultra Scale +	CXP2.0	12.5Gbps	VCU118	Encrypted netlist, Source code
Versal AI Core	CXP2.0 Available on request	12.5Gbps	Available on request	Encrypted netlist, Source code
Versal Prime	CXP2.0 Available on request	12.5Gbps	Available on request	Encrypted netlist, Source code

Altera FPGA

Device Family	Support	Maximum Links Speed	Evaluation Boards Reference Design	Code Options
Altera Cyclone V GX	CXP2.0 Available on request	6.25Gbps	DK-DEV-5CGXC7NES	Encrypted netlist, Source code
Altera Cyclone V SX	CXP2.0 Available on request	6.25Gbps	Available on request	Encrypted netlist, Source code
Altera Cyclone 10	CXP2.0	12.5Gbps	DK-DEV-10CX220-A	Encrypted netlist, Source code
Altera Stratix V GX	CXP2.0 Available on request	12.5Gbps	DK-DEV-5SGXEA7N	Encrypted netlist, Source code
Altera Stratix 10 GX	CXP2.0	12.5Gbps	Available on request	Encrypted netlist, Source code
Altera Arria V GZ	CXP2.0 Available on request	6.25Gbps	Available on request	Encrypted netlist, Source code
Altera Arria V GX	CXP2.0 Available on request	6.25Gbps	DK-START-5AGXB3N	Encrypted netlist, Source code
Altera Arria V SX	CXP2.0 Available on request	6.25Gbps	Available on request	Encrypted netlist, Source code
Altera Arria 10 SX	CXP2.0	12.5Gbps	DK-START-10AS066	Encrypted netlist, Source code
Altera Arria 10 GX	CXP2.0	12.5Gbps	DK-DEV-10AX115	Encrypted netlist, Source code

Microsemi FPGA

Device Family	Support	Maximum Links Speed	Evaluation Boards Reference Design	Code Options
PolarFire MPF100T	CXP2.0	12.5Gbps	DVP-102-000521-001	Source code
PolarFire MPF200T	CXP2.0	12.5Gbps	Available on request	Source code
PolarFire MPF300T	CXP2.0	12.5Gbps	DVP-102-000481-001	Source code

Note:

1. The Device CXP IP is available for additional FPGA devices upon request.
2. Reference design for additional evaluation boards or customized HW is available on request.

CORE DETAILS

- Language: Verilog HDL
- Soft IP core: available as RTL- encrypted netlist and as source code
- Support of AMD Xilinx®, Intel® and Microsemi® FPGAs
- Highly configurable logic providing operational flexibility and customization
- Integrated synchronization logic for clock domain crossing providing robust designing
- Supports a wide, continuous range of operating clock speeds for design versatility
- Includes a comprehensive set of parameters for utilization optimization
- Integrated internal packing/un-packing logic for communication and streaming
- Integrated internal logic for latency optimization complying with the CXP2.0 protocol
- Integrated internal error management logic
- Provided with comprehensive documentation package

PERFORMANCE AND RESOURCE UTILIZATION

The IP logic's resource utilization and performance vary according to the configuration and parameterization of the IP.
The following tables present the performance and resource utilization of the Device CXP IP core for the default configuration provided.

Xilinx AMD FPGA

Device Family	LUT	FFs	BRAMs	Max Video Stream Clock	Max Control Channel Clock
Artix 7, single link, single stream	4k	6k	15	230MHz	125MHz
Artix 7, quad link, single stream	12k	16k	38	220MHz	125MHz
Artix Ultrascale +, single link, single stream	4k	6k	15	350MHz	175MHz
Artix Ultrascale +, quad link, single stream	12k	16k	38	350MHz	175MHz
Kintex 7, single link, single stream	4k	6k	15	300MHz	175MHz
Kintex 7, quad link, single stream	12k	16k	38	300MHz	175MHz
Kintex Ultra Scale, single link, single stream	4k	6k	15	350MHz	175MHz
Kintex Ultra Scale, quad link, single stream	12k	16k	38	350MHz	175MHz
Kintex Ultra Scale +, single link, single stream	4k	6k	15	350MHz	175MHz
Kintex Ultra Scale +, quad link, single stream	12k	16k	38	350MHz	175MHz
Virtex 7, single link, single stream	4k	6k	15	300MHz	175MHz
Virtex 7, quad link, single stream	12k	16k	38	300MHz	175MHz
Virtex Ultra Scale, single link, single stream	4k	6k	15	350MHz	175MHz
Virtex Ultra Scale, quad link, single stream	12k	16k	38	350MHz	175MHz
Virtex Ultra Scale +, single link, single stream	4k	6k	15	350MHz	175MHz
Virtex Ultra Scale +, quad link, single stream	12k	16k	38	350MHz	175MHz
ZYNQ 7000, single link single stream	4k	6k	15	300MHz	175MHz
ZYNQ 7000, quad link single stream	12k	16k	15	300MHz	175MHz
ZYNQ Ultra Scale +, single link, single stream	4k	6k	15	350MHz	175MHz
ZYNQ Ultra Scale +, quad link, single stream	12k	16k	38	350MHz	175MHz

Altera FPGA

Device Family	ALMs	FFs	M20Ks	Max Video Stream Clock	Max Control Channel Clock
Altera Cyclone 10, single link, single stream	3k	6k	22	350MHz	175MHz
Altera Cyclone 10, quad link, single stream	10k	14k	62	350MHz	175MHz
Altera Stratix 10 GX, single link, single stream	3k	6k	22	350MHz	175MHz
Altera Stratix 10 GX, quad link, single stream	10k	14k	62	350MHz	175MHz
Altera Arria 10 SX, single link, single stream	3k	6k	22	350MHz	175MHz
Altera Arria 10 SX, quad link, single stream	10k	14k	62	350MHz	175MHz
Altera Arria 10 GX, single link, single stream	3k	6k	22	350MHz	175MHz
Altera Arria 10 GX, quad link, single stream	10k	14k	62	350MHz	175MHz

Microsemi FPGA

Device Family	LUT	FFs	BRAMs	Max Video Stream Clock	Max Control Channel Clock
PolarFire MPF100T, single link, single stream	9k	7k	24	300MHz	150MHz
PolarFire MPF100T, quad link, single stream	12k	13k	56	300MHz	150MHz
PolarFire MPF200T, single link, single stream	9k	7k	24	300MHz	150MHz
PolarFire MPF200T, quad link, single stream	12k	13k	56	300MHz	150MHz
PolarFire MPF300T, single link, single stream	9k	7k	24	300MHz	150MHz
PolarFire MPF300T, quad link, single stream	12k	13k	56	300MHz	150MHz

LICENSING OPTIONS

The evaluation license of the Device CXP IP core is available for a 3-month free evaluation period.

The operational IP core is available with 3 types of licenses. The license options are:

Encrypted Netlist

This option includes KAYA's IP core coupled with Xilinx or Altera license with unlimited implementation available.

The license provides a fully operational design for the FPGA family device of the customer's choice. Both the IP core and the transceivers' configuration logic are provided encrypted. The migration of the IP core to an additional FPGA family device is available under a migration fee.

The license can be either node-locked or a server. It is generated for a single working station – a single PC station in case of node-locked license and 1 seat in case of server.

The support hours that are included in the package - 10 hours.

Source Code

This option includes the entire HDL sources of the IP. The package also includes the source code of the transceivers' configuration, based on the FPGA family device of the customer's choice, and is entirely open for reference. The IP core is fully unlimited and does not require a compilation license.

This option requires non-compete and non-IP-resell agreements signature.

The support hours that are included in the package – 24 hours.

Free Encrypted Netlist

This option is available for projects based on KAYA instruments' products (e.g., FMC mezzanine cards, custom Hardware manufactured by KAYA, etc.). The IP includes an authentication logic which verifies integration with KAYA's Hardware. Under this option, the encrypted version of the IP is provided free of cost.

The license can be either node-locked or a server. It is generated for a single working station – a single PC station in case of node-locked license and 1 seat in case of server.

No support hours are included in this option.

WARRANTY AND MAINTENANCE

Warranty

The Device CXP IP core includes a warranty of 12 months after the purchase. The warranty covers any repairs, updates, or exchanges if the IP does not function as originally described or intended. Once the warranty period expires, it can be extended by purchasing the maintenance package.

Please note that the warranty period must be continuous and renewed without respite. In case the warranty period is interrupted the renewal of the warranty will include an additional fee.

Maintenance

The extended maintenance package is available to acquire during the warranty period. The maintenance package includes the following services and support:

- Warranty package
- Free routine updates of the IP core due to logic upgrades, performance improvements and bug fixes
- An additional 10 hours of technical support upon request
- Free license migration to additional running machine

Please note that the maintenance period must be continuous and renewed without respite. In case the maintenance period is interrupted the renewal of the maintenance will include an additional fee.

DELIVERABLES

- CoaXPress FPGA Device IP Core
- Reference design based on the relevant Vendor's evaluation board
- Configuration of the transceivers
- An auxiliary RTL logic of the operational Bootstrap registers
- An example of an operational XML file & XML conversion app
- Auxiliary logic blocks and applicable bridges
- Comprehensive usage example
- A comprehensive package of documentation
- A 12-month warranty

COMPATIBILITY

KAYA Vision develops and maintains compatibility and interfaces for the most common and advanced vision image processing libraries and applications. We ensure seamless integration with major platforms to provide users with a flexible and convenient development environment, minimize integration effort, and accelerate time to deployment.

Supported vision standards:

CoaXPress GEN<i>CAM GENTL

Please check our website for an up-to-date list of other supported libraries and software package

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KAYA VISION

Have questions about pricing, availability, documentation, or custom options?
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