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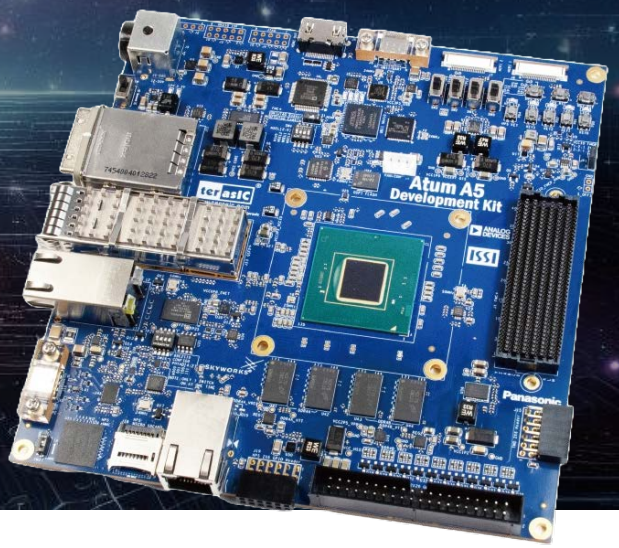
Atum A5 Development Kit

Higher Speed, Richer Interfaces with Cutting Edge AI features based on Intel® Agilex™ 5 SoC FPGA !



2024年12月23日 出荷開始しました。型番 P0775

The Atum A5 Development Kit is Terasic' s first dev kit in the Altera® Agilex™ 5 FPGA portfolio. Powered by the largest Agilex™ 5 SoC FPGA with 656K LEs, the Atum A5 Development Kit is an out-of-the-box platform for midrange AI and vision application development.

With a rich set of interfaces ranging from 2.5G Ethernet, high-speed DDR4, QSFP+, PCIe Gen 3 x4 and FMC+ connectors to MIPI connector and HDMI, the Atum A5 excels in a wide range of applications, including industrial networking, AI, embedded vision, medical and healthcare, video applications, and various other I/O expansion and high-speed applications!

Key Benefits

FPGA

Altera® Agilex™ 5 E-Series with 656K LEs and consisting of HPS with 2 xA55 and 2 xA76. Core Speed Grade: -4S A5ED065BB32AE4SR0

Software Support

Support Linux BSP for HPS development

Memory Interface

Two On-board DDR4 banks with 32-bit data bus (no ECC). One shared with HPS

Multi-media

One HDMI OUT (ADV7513; Support 1080P) for video output

Connectivity

HPC FMC+ (12 transceivers), 2 x20 GPIO and 2 x6 TMD connector one each for expansion

Camera

Two 2-lane MIPI connectors for vision application

Transceivers

2.5G Ethernet, PCIe cabling Gen 3 x4 socket and One QSFP+ for high speed communication

HPS Interface

Support USB 3.1 Gen 1, USB to UART, 8GB eMMC/MicroSD socket, 2 x6 GPIO header and Gigabit interface for HPS communication

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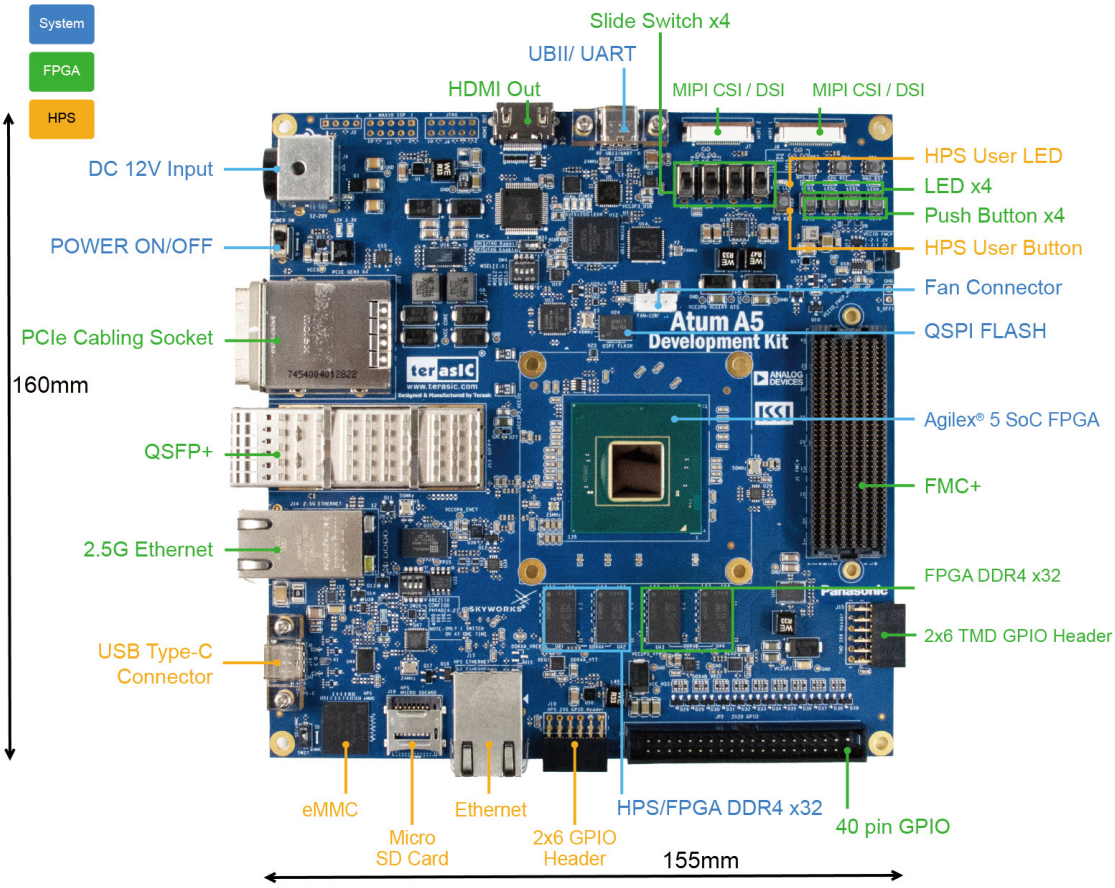
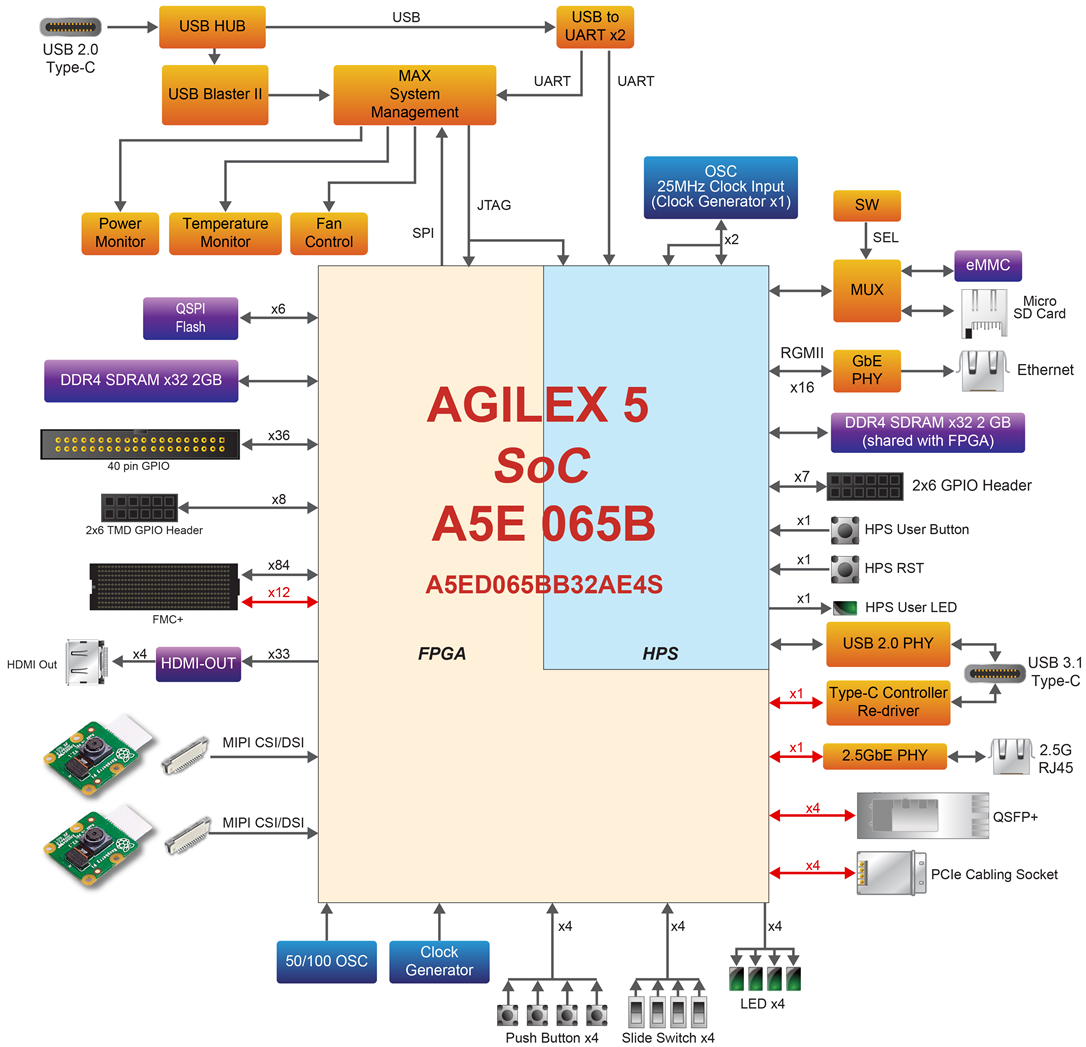
Atum A5ボード レイアウトとブロック図





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